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*Liu, M.-K.;*

Communications, IEEE Transactions on, Volume: 40, Issue: 9, Sept. 1992  
Pages:1522 - 1531

[\[Abstract\]](#) [\[PDF Full-Text \(692 KB\)\]](#) **IEEE JNL**

**2 Rate-proportional servers: a design methodology for fair queueing algorithms**

*Stiliadis, D.; Varma, A.;*

Networking, IEEE/ACM Transactions on, Volume: 6, Issue: 2, April 1998  
Pages:164 - 174

[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) **IEEE JNL**

**3 Synchronous emulation of asynchronous circuits**

*O'Leary, J.; Brown, G.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on, Volume: 16, Issue: 2, Feb. 1997  
Pages:205 - 209

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) **IEEE JNL**

**4 Novel techniques for performance optimisation of DECT receivers with non-linear front-end**

*Safavi, S.; Lopes, L.B.;*

Vehicular Technology Conference, 1996. 'Mobile Technology for the Human Race' IEEE 46th, Volume: 2, 28 April-1 May 1996  
Pages:824 - 828 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(508 KB\)\]](#) **IEEE CNF**

**5 Design methodology of a 200 MHz superscalar macroprocessor: SH-**  
*Hattori, T.; Nitta, Y.; Seki, M.; Narita, S.; Uchiyama, K.; Takahashi, T.; Satom R.;*  
Design Automation Conference, 1998. Proceedings , 15-19 June 1998  
Pages:246 - 249

[\[Abstract\]](#) [\[PDF Full-Text \(412 KB\)\]](#) [IEEE CNF](#)

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**6 A dual-loop delay-locked loop using multiple voltage-controlled delay lines**

*Yeon-Jae Jung; Seung-Wook Lee; Daeyun Shim; Wonchan Kim; Changhyun K Soo-In Cho;*  
Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 5 , May 2001  
Pages:784 - 791

[\[Abstract\]](#) [\[PDF Full-Text \(236 KB\)\]](#) [IEEE JNL](#)

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**7 Digital phased array beamforming using single-bit delta-sigma conversion with non-uniform oversampling**

*Kozak, M.; Karaman, M.;*  
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , Volu 48 , Issue: 4 , July 2001  
Pages:922 - 931

[\[Abstract\]](#) [\[PDF Full-Text \(1684 KB\)\]](#) [IEEE JNL](#)

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**8 Design methodology for synthesizing clock distribution networks exploiting nonzero localized clock skew**

*Neves, J.L.; Friedman, E.G.;*  
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 4 , Issue: 2 , June 1996  
Pages:286 - 291

[\[Abstract\]](#) [\[PDF Full-Text \(724 KB\)\]](#) [IEEE JNL](#)

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**9 Importance of CAD tools and methodologies in high speed CPU desi**  
*Tago, H.; Hashimoto, K.; Ikumi, N.; Nagamatsu, M.; Suzuoki, M.; Yamamoto,*  
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia South Pacific , 25-28 Jan. 2000  
Pages:631 - 633

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**10 Priority inheritance and ceilings for distributed mutual exclusion**

*Mueller, F.;*  
Real-Time Systems Symposium, 1999. Proceedings. The 20th IEEE , 1-3 Dec.

Pages:340 - 349

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) [IEEE CNF](#)

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**11 Minimizing power dissipation in non-zero skew-based clock distribution networks**

*Neves, J.L.; Friedman, E.G.;*  
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , Volume: 3 , 28 April-3 May 1995

Pages:1576 - 1579 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(484 KB\)\]](#) [IEEE CNF](#)

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**12 Contention resolution with bounded delay**

*Paterson, M.; Srinivasan, A.;*

Foundations of Computer Science, 1995. Proceedings., 36th Annual Symposium on, 23-25 Oct. 1995

Pages:104 - 113

[\[Abstract\]](#) [\[PDF Full-Text \(1020 KB\)\]](#) [IEEE CNF](#)

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**13 Circuit synthesis of clock distribution networks based on non-zero skew**

*Neves, J.L.; Friedman, E.G.;*

Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on, Volume: 4, 30 May-2 June 1994

Pages:175 - 178 vol.4

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**14 Synthesizing distributed buffer clock trees for high performance AS**

*Neves, J.L.; Friedman, E.G.;*

ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International, 19-23 Sept. 1994

Pages:126 - 129

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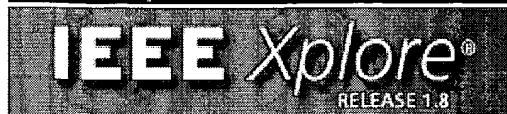
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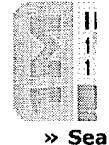
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**1 Hardware and software cache prefetching techniques for MPEG benchmarks**

Zucker, D.F.; Lee, R.B.; Flynn, M.J.;  
Circuits and Systems for Video Technology, IEEE Transactions on, Volume: 10, Issue: 5, Aug. 2000  
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**2 Debugging aids for systems-on-a-chip**

Bannatyne, R.;  
Northcon/98 Conference Proceedings, 21-23 Oct. 1998  
Pages: 159 - 163

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Tago, H.; Hashimoto, K.; Ikumi, N.; Nagamatsu, M.; Suzuki, M.; Yamamoto, T.;  
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia South Pacific, 25-28 Jan. 2000  
Pages: 631 - 633

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) **IEEE CNF**

**4 A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation**

Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.;  
Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, M.; Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R.; Takasuga, T.; Hasegawa, A.;  
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International, 5-7 Feb. 1998  
Pages: 288 - 289, 447

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**Accession number & update**

6450532, B2000-02-6150M-036, C2000-02-5640-031; 19991201.

**Title**Circuit **emulation** over IP networks.**Author(s)**

Noro-R; Hamdi-M; Hubaux-J-P; Ed. by Touch-J-D; Sterbenz-J-P-G.

**Author affiliation**

Inst for Comput Commun &amp; Applications, Swiss Fed Inst of Technol, Lausanne, Switzerland.

**Source**Proceedings of Conference on Protocols for High Speed Networks, Salem, MA, USA, 25-27 Aug. 1999.  
In: p.187-201, 2000.**ISSN**

ISBN: 0-7923-8690-6.

**Publication year**

2000.

**Language**

EN.

**Publication type**

CPP Conference Paper.

**Treatment codes**

P Practical; T Theoretical or Mathematical.

**Abstract**

Recent developments in transmission and switching technology has made available low-cost gigabit **network** capacity for packet-based WAN (e.g., IP over WDM), that will not require the intermediate SONET/SDH multiplexing layer. For competitive operators that want to minimize their investment by deploying native IP over WDM networks, circuit **emulation** over IP gives support to the important class of legacy circuit-based equipment (e.g., T1/E1 multiplexers), which otherwise will require the deployment of an expensive telecommunication infrastructure, including SONET/SDH equipment. At the user interface, circuit **emulation** is required to maintain the same service of a circuit-based **network**, including synchronization and structured data delivery. In this paper we design the algorithm and the protocol that provide these two features. First, we identify the protocols and mechanisms used in the Internet and their ability to be used for circuit **emulation**. Second, we address the problem of synchronization and we propose an algorithm for efficient source **clock** recovery and handling of **delay** variations. Finally, we show through simulations that circuit **emulation** over IP provides the needed service performance at the user interface. (14 refs).

**Descriptors**[circuit-switching](#); [packet-switching](#); [protocols](#); [synchronisation](#);  
[wavelength-division-multiplexing](#); [wide-area-networks](#).**Keywords**

circuit **emulation**; IP networks; packet based WAN; gigabit **network** capacity; WDM; legacy circuit based equipment; synchronization; structured data delivery; protocol; Internet; source **clock** recovery; **delay** variation; simulations; service performance; user interface.

**Classification codes**

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B6210L (Computer communications).  
B6150C (Communication switching).  
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TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

**INVENTOR-INFORMATION:**

NAME	CITY	STATE	COUNTRY	RULE-47
Hoare, Raymond R. II	Pittsburgh	PA	US	
Ahn, Jiyong	Pittsburgh	PA	US	
Graves, Jesse	Pittsburgh	PA	US	

US-CL-CURRENT: 703/17

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TITLE: Methods and apparatus for device access fairness in fibre channel arbitrated loop systems

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	
White, Michael L.	Oak Harbor	WA	US	
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INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mies, Carl	Snohomish	WA	US	
Warren, Bruce Gregory	Poulsbo	WA	US	

US-CL-CURRENT: 370/406

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NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Hammond-Doel, Thomas	Everett	WA	US	
White, Michael L.	Oak Harbor	WA	US	

US-CL-CURRENT: 370/401

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Drawn D
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 4. Document ID: US 20040081187 A1

L26: Entry 4 of 7

File: PGPB

Apr 29, 2004

PGPUB-DOCUMENT-NUMBER: 20040081187

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040081187 A1

TITLE: Methods and apparatus for switching fibre channel arbitrated loop systems

PUBLICATION-DATE: April 29, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodman, William P.	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	
White, Michael L.	Oak Harbor	WA	US	
Eng, Warren	Renton	WA	US	

US-CL-CURRENT: 370/419

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Drawn D
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5. Document ID: US 20040081186 A1

L26: Entry 5 of 7

File: PGPB

Apr 29, 2004

PGPUB-DOCUMENT-NUMBER: 20040081186

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040081186 A1

TITLE: Methods and apparatus for switching Fibre Channel Arbitrated Loop devices

PUBLICATION-DATE: April 29, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
White, Michael L.	Oak Harbor	WA	US	
Eng, Warren	Renton	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	

US-CL-CURRENT: 370/419

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMNC	Drawn D
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 6. Document ID: US 6377561 B1

L26: Entry 6 of 7

File: USPT

Apr 23, 2002

US-PAT-NO: 6377561

DOCUMENT-IDENTIFIER: US 6377561 B1

TITLE: Data communication satellite system and method of carrying multi-media traffic

DATE-ISSUED: April 23, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Black; Colin J.	St. Lazare			CA
Takats; Peter	Ile Perrot			CA
Cote; Martin	Montreal			CA
Le-Ngoc; Tho T.	Anjou			CA

US-CL-CURRENT: 370/330

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMNC	Drawn D
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 7. Document ID: US 4486827 A

L26: Entry 7 of 7

File: USPT

Dec 4, 1984

US-PAT-NO: 4486827

DOCUMENT-IDENTIFIER: US 4486827 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Microprocessor apparatus

DATE-ISSUED: December 4, 1984

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shima; Masatoshi	Santa Clara	CA		
Faggin; Federico	Cupertino	CA		
Ungermann; Ralph K.	Los Altos	CA		

US-CL-CURRENT: 710/261

Full	Title	Citation	Front	Review	Classification	Date	Reference	Searcher	Assignee	Claims	KWMC	Drawn D
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Term	Documents
CYCLE	607778
CYCLES	298482
(25 AND CYCLE).PGPB,USPT.	7
(L25 AND CYCLE ).PGPB,USPT.	7

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**Hit List**

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

**Search Results - Record(s) 1 through 8 of 8 returned.**

1. Document ID: US 5426765 A

**Using default format because multiple data bases are involved.**

L16: Entry 1 of 8

File: USPT

Jun 20, 1995

US-PAT-NO: 5426765

DOCUMENT-IDENTIFIER: US 5426765 A

TITLE: Multiprocessor cache arbitration

DATE-ISSUED: June 20, 1995

**INVENTOR-INFORMATION:**

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stevens; Jeffrey C.	Spring	TX		
Jackson; Mike T.	Houston	TX		
Tipley; Roger E.	Houston	TX		
Ramsey; Jens K.	Houston	TX		
Olarig; Sompong	Cypress	TX		
Kelly; Philip C.	Houston	TX		

US-CL-CURRENT: 711/131; 711/146, 711/167

Full	Title	Citation	Front	Review	Classification	Date	Reference	Search	Search	Claims	KOMC	Draw. D
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2. Document ID: US 5097437 A

L16: Entry 2 of 8

File: USPT

Mar 17, 1992

US-PAT-NO: 5097437

DOCUMENT-IDENTIFIER: US 5097437 A

TITLE: Controller with clocking device controlling first and second state machine controller which generate different control signals for different set of devices

DATE-ISSUED: March 17, 1992

**INVENTOR-INFORMATION:**

NAME	CITY	STATE	ZIP CODE	COUNTRY
Larson; Ronald J.	Minneapolis	MN	55419	

US-CL-CURRENT: 712/245; 703/25

Full	Title	Citation	Front	Review	Classification	Date	Reference	Search	Search	Claims	KOMC	Draw. D
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3. Document ID: US 5053947 A

L16: Entry 3 of 8

File: USPT

Oct 1, 1991

US-PAT-NO: 5053947

DOCUMENT-IDENTIFIER: US 5053947 A

TITLE: Extended multistation bus system and method

DATE-ISSUED: October 1, 1991

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heibel; John T.	Columbus	OH		
Savarda; Raymond R.	Centerburg	OH		

US-CL-CURRENT: 709/237; 370/389, 370/438[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Abstracts](#) [Inventors](#) [Claims](#) [KIMC](#) [Draw. D](#) 4. Document ID: US 4137565 A

L16: Entry 4 of 8

File: USPT

Jan 30, 1979

US-PAT-NO: 4137565

DOCUMENT-IDENTIFIER: US 4137565 A

TITLE: Direct memory access module for a controller

DATE-ISSUED: January 30, 1979

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Gillett; Kenneth	Redondo Beach	CA		
Holt; Charles P.	Palos Verdes	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Palos Verdes	CA		
Criswell; Thomas	Venice	CA		
Hall; Warren L.	Fairport	NY		

US-CL-CURRENT: 710/22[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Abstracts](#) [Inventors](#) [Claims](#) [KIMC](#) [Draw. D](#) 5. Document ID: US 4131945 A

L16: Entry 5 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131945

DOCUMENT-IDENTIFIER: US 4131945 A

TITLE: Watch dog timer module for a controller

DATE-ISSUED: December 26, 1978

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Richardson; Philip	Pacific Palisades	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Fairport	NY		
Criswell; Thomas	Venice	CA		

US-CL-CURRENT: 714/55

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Abstract	Claims	KMC	Drawn D
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 6. Document ID: US 4131944 A

L16: Entry 6 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131944

DOCUMENT-IDENTIFIER: US 4131944 A

TITLE: System bus module for a controller

DATE-ISSUED: December 26, 1978

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Hall; Warren L.	Palos Verdes	CA		

US-CL-CURRENT: 710/107

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Abstract	Claims	KMC	Drawn D
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 7. Document ID: US 4131942 A

L16: Entry 7 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131942

DOCUMENT-IDENTIFIER: US 4131942 A

TITLE: Non-volatile storage module for a controller

DATE-ISSUED: December 26, 1978

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gillett; Kenneth	Redondo Beach	CA		
Steiner; Edward L.	Macedon	NY		
Fiske; Kenton W.	Fairport	NY		
Davis; Kenneth A.	Honeoye Falls	NY		
Kukucka; William P.	Webster	NY		
Criswell; Thomas	Venice	CA		
Richardson; Philip	Pacific Palisades	CA		

US-CL-CURRENT: 714/22

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Abstract](#) [View Document](#) [Claims](#) [KIMC](#) [Drawn D](#)

8. Document ID: US 3582628 A

L16: Entry 8 of 8

File: USPT

Jun 1, 1971

US-PAT-NO: 3582628

DOCUMENT-IDENTIFIER: US 3582628 A

TITLE: ANALOG-DIGITAL COMPUTER INTERCONNECTION SYSTEM

DATE-ISSUED: June 1, 1971

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brussolo; John A.	Ann Arbor	MI		

US-CL-CURRENT: 708/2; 708/6, 708/817, 708/835, 708/840

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Abstract](#) [View Document](#) [Claims](#) [KIMC](#) [Drawn D](#)

[Clear](#) [Generate Collection](#) [Print](#) [Fwd Refs](#) [Bkwd Refs](#) [Generate OACS](#)

Term	Documents
CLOCK	272984
CLOCKS	53522
(15 AND CLOCK).PGPB,USPT.	8
(L15 AND CLOCK ).PGPB,USPT.	8

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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

**Search Results - Record(s) 1 through 4 of 4 returned.**

1. Document ID: US 4137565 A

**Using default format because multiple data bases are involved.**

L13: Entry 1 of 4

File: USPT

Jan 30, 1979

US-PAT-NO: 4137565

DOCUMENT-IDENTIFIER: US 4137565 A

TITLE: Direct memory access module for a controller

DATE-ISSUED: January 30, 1979

**INVENTOR-INFORMATION:**

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Gillet; Kenneth	Redondo Beach	CA		
Holt; Charles P.	Palos Verdes	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Palos Verdes	CA		
Criswell; Thomas	Venice	CA		
Hall; Warren L.	Fairport	NY		

US-CL-CURRENT: 710/22

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Assignments	Claims	KOMC	Drawn D.
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2. Document ID: US 4131945 A

L13: Entry 2 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131945

DOCUMENT-IDENTIFIER: US 4131945 A

TITLE: Watch dog timer module for a controller

DATE-ISSUED: December 26, 1978

**INVENTOR-INFORMATION:**

NAME	CITY	STATE	ZIP CODE	COUNTRY
Richardson; Philip	Pacific Palisades	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		

Fiske; Kenton W.	Fairport	NY
Criswell; Thomas	Venice	CA

US-CL-CURRENT: 714/55

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Assignments	Claims	KOMC	Drawn D
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3. Document ID: US 4131944 A

L13: Entry 3 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131944

DOCUMENT-IDENTIFIER: US 4131944 A

TITLE: System bus module for a controller

DATE-ISSUED: December 26, 1978

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Hall; Warren L.	Palos Verdes	CA		

US-CL-CURRENT: 710/107

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Assignments	Claims	KOMC	Drawn D
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4. Document ID: US 4131942 A

L13: Entry 4 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131942

DOCUMENT-IDENTIFIER: US 4131942 A

TITLE: Non-volatile storage module for a controller

DATE-ISSUED: December 26, 1978

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gillett; Kenneth	Redondo Beach	CA		
Steiner; Edward L.	Macedon	NY		
Fiske; Kenton W.	Fairport	NY		
Davis; Kenneth A.	Honeoye Falls	NY		
Kukucka; William P.	Webster	NY		
Criswell; Thomas	Venice	CA		
Richardson; Philip	Pacific Palisades	CA		

US-CL-CURRENT: 714/22

## Hit List

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

### Search Results - Record(s) 1 through 17 of 17 returned.

1. Document ID: US 20020178427 A1

**Using default format because multiple data bases are involved.**

L33: Entry 1 of 17

File: PGPB

Nov 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020178427

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020178427 A1

TITLE: Method for improving timing behavior in a hardware logic emulation system

PUBLICATION-DATE: November 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ding, Cheng-Liang	Cupertino	CA	US	
Freeman, Thomas H.	Sunnyvale	CA	US	
Chao, Liang-Fang	Cupertino	CA	US	
Ben-Tzur, Tzvi	Sunnyvale	CA	US	

US-CL-CURRENT: 716/12

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. D
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2. Document ID: US 20020133325 A1

L33: Entry 2 of 17

File: PGPB

Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020133325

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020133325 A1

TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Hoare, Raymond R. II	Pittsburgh	PA	US	
Ahn, Jiyong	Pittsburgh	PA	US	
Graves, Jesse	Pittsburgh	PA	US	

US-CL-CURRENT: 703/17

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Draw. De](#)

3. Document ID: US 20010036188 A1

L33: Entry 3 of 17

File: PGPB

Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010036188

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010036188 A1

TITLE: Multi-service circuit for telecommunications

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Carlsson, Dan	Hasselby		SE	

US-CL-CURRENT: 370/395.4; 370/465, 370/535

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Draw. De](#)

4. Document ID: US 6377561 B1

L33: Entry 4 of 17

File: USPT

Apr 23, 2002

US-PAT-NO: 6377561

DOCUMENT-IDENTIFIER: US 6377561 B1

TITLE: Data communication satellite system and method of carrying multi-media traffic

DATE-ISSUED: April 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Black; Colin J.	St. Lazare			CA
Takats; Peter	Ile Perrot			CA
Cote; Martin	Montreal			CA
Le-Ngoc; Tho T.	Anjou			CA

US-CL-CURRENT: 370/330

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Draw. De](#)

5. Document ID: US 6256308 B1

L33: Entry 5 of 17

File: USPT

Jul 3, 2001

US-PAT-NO: 6256308

DOCUMENT-IDENTIFIER: US 6256308 B1

TITLE: Multi-service circuit for telecommunications

DATE-ISSUED: July 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Carlsson; Dan	Hasselby			SE

US-CL-CURRENT: 370/395.43; 370/395.5, 370/465, 370/535

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Searcher](#) [Assignee](#) [Claims](#) [KMC](#) [Drawn](#) [De](#)

6. Document ID: US 5893049 A

L33: Entry 6 of 17

File: USPT

Apr 6, 1999

US-PAT-NO: 5893049

DOCUMENT-IDENTIFIER: US 5893049 A

TITLE: Rapid response voltage threshold determination circuit for electrophysiology diagnostic device

DATE-ISSUED: April 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 702/71; 702/193, 714/735, 714/736

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Searcher](#) [Assignee](#) [Claims](#) [KMC](#) [Drawn](#) [De](#)

7. Document ID: US 5835751 A

L33: Entry 7 of 17

File: USPT

Nov 10, 1998

US-PAT-NO: 5835751

DOCUMENT-IDENTIFIER: US 5835751 A

TITLE: Structure and method for providing reconfigurable emulation circuit

DATE-ISSUED: November 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 716/16; 327/39

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMPC	Drawn D
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8. Document ID: US 5793356 A

L33: Entry 8 of 17

File: USPT

Aug 11, 1998

US-PAT-NO: 5793356

DOCUMENT-IDENTIFIER: US 5793356 A

TITLE: System and method for the software emulation of a computer joystick

DATE-ISSUED: August 11, 1998

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Pierce; John G.	Vashon	WA		
Suzuki; Hajime	Kanagawa-ken			JP
Kash; Richard B.	Los Altos Hills	CA		

US-CL-CURRENT: 345/161; 345/157, 463/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMPC	Drawn D
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9. Document ID: US 5754828 A

L33: Entry 9 of 17

File: USPT

May 19, 1998

US-PAT-NO: 5754828

DOCUMENT-IDENTIFIER: US 5754828 A

**\*\* See image for Certificate of Correction \*\***

TITLE: System and method for positional control device data source selection

DATE-ISSUED: May 19, 1998

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Dean; Daniel	Issaquah	WA		
Davis; Jeffrey A.	Bothell	WA		

US-CL-CURRENT: 703/24

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMPC	Drawn D
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10. Document ID: US 5724558 A

L33: Entry 10 of 17

File: USPT

Mar 3, 1998

US-PAT-NO: 5724558

DOCUMENT-IDENTIFIER: US 5724558 A

TITLE: System and method for dynamic data packet configuration

DATE-ISSUED: March 3, 1998

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Suzuki; Hajime	Kanagawa-ken			JP

US-CL-CURRENT: 703/21; 345/156, 345/161, 345/168, 703/24, 710/20, 710/58, 712/227,  
719/321[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Abstracts](#) | [Patents](#) | [Claims](#) | [KOMC](#) | [Drawn D](#) 11. Document ID: US 5716381 A

L33: Entry 11 of 17

File: USPT

Feb 10, 1998

US-PAT-NO: 5716381

DOCUMENT-IDENTIFIER: US 5716381 A

TITLE: Electrophysiology diagnostic device including variable capacitance emulation and voltage threshold determination circuits

DATE-ISSUED: February 10, 1998

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 607/8; 607/5, 607/7[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Abstracts](#) | [Patents](#) | [Claims](#) | [KOMC](#) | [Drawn D](#) 12. Document ID: US 5694949 A

L33: Entry 12 of 17

File: USPT

Dec 9, 1997

US-PAT-NO: 5694949

DOCUMENT-IDENTIFIER: US 5694949 A

TITLE: Variable capacitance emulation circuit for electrophysiology diagnostic device

DATE-ISSUED: December 9, 1997

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 128/897; 323/354

Full	Title	Citation	Front	Review	Classification	Date	Reference	Searcher	Searcher	Claims	KWIC	Drawn D
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 13. Document ID: US 5682353 A

L33: Entry 13 of 17

File: USPT

Oct 28, 1997

US-PAT-NO: 5682353

DOCUMENT-IDENTIFIER: US 5682353 A

TITLE: Self adjusting sense amplifier clock delay circuit

DATE-ISSUED: October 28, 1997

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eitan; Boaz	Ra'anana			IL
Petersen; Larry Willis	Pocatello	ID		
Slezak; Yaron	Kiriat Motzkin			IL

US-CL-CURRENT: 365/233; 365/185.21, 365/194, 365/233.5

Full	Title	Citation	Front	Review	Classification	Date	Reference	Searcher	Searcher	Claims	KWIC	Drawn D
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 14. Document ID: US 5649167 A

L33: Entry 14 of 17

File: USPT

Jul 15, 1997

US-PAT-NO: 5649167

DOCUMENT-IDENTIFIER: US 5649167 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Methods for controlling timing in a logic emulation system

DATE-ISSUED: July 15, 1997

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 703/23

Full	Title	Citation	Front	Review	Classification	Date	Reference	Searcher	Searcher	Claims	KWIC	Drawn D
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15. Document ID: US 5628686 A

L33: Entry 15 of 17

File: USPT

May 13, 1997

US-PAT-NO: 5628686

DOCUMENT-IDENTIFIER: US 5628686 A

TITLE: Apparatus and method for bidirectional data communication in a game port

DATE-ISSUED: May 13, 1997

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Suzuki; Hajime	Kanagawa-ken			JP

US-CL-CURRENT: 463/36[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Document](#) [Assignment](#) [Claims](#) [KUDC](#) [Drawn D](#) 16. Document ID: US 5475830 A

L33: Entry 16 of 17

File: USPT

Dec 12, 1995

US-PAT-NO: 5475830

DOCUMENT-IDENTIFIER: US 5475830 A

TITLE: Structure and method for providing a reconfigurable emulation circuit without hold time violations

DATE-ISSUED: December 12, 1995

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 716/16; 716/17, 716/7[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Document](#) [Assignment](#) [Claims](#) [KUDC](#) [Drawn D](#) 17. Document ID: US 5452239 A

L33: Entry 17 of 17

File: USPT

Sep 19, 1995

US-PAT-NO: 5452239

DOCUMENT-IDENTIFIER: US 5452239 A

TITLE: Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system

DATE-ISSUED: September 19, 1995

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dai; Wei-Jin	Cupertino	CA		
Galbiati, III; Louis	Mountain View	CA		
Varghese; Joseph	Sunnyvale	CA		
Bui; Dam V.	Milpitas	CA		
Sample; Stephen P.	Mountain View	CA		

US-CL-CURRENT: 703/19; 714/725, 716/17

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Abstract	Claims	KV/MC	Draw. D
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Term	Documents
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PROGRAMMABLES	10
(32 AND PROGRAMMABLE).PGPB,USPT.	17
(L32 AND PROGRAMMABLE ).PGPB,USPT.	17

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